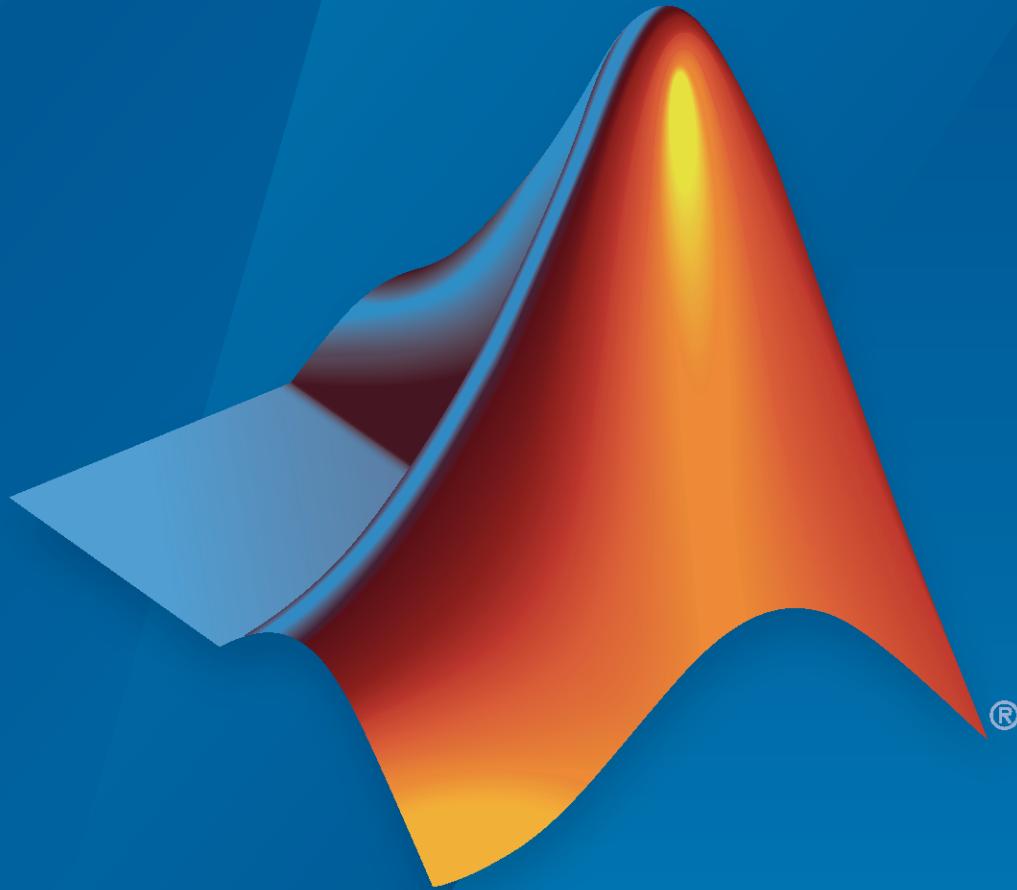


DSP HDL Toolbox™ Release Notes



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### *DSP HDL Toolbox™ Release Notes*

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<b>Model and simulate hardware-optimized implementations of DSP algorithms</b> .....	<b>1-2</b>
<b>Enable gigasamples-per-second (GSPS) throughput by using optional parallel processing</b> .....	<b>1-2</b>
<b>Generate HDL code for FPGAs, ASICs, and SoCs (requires HDL Coder)</b> .....	<b>1-2</b>



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**Version: 1.0**

**New Features**

## **Model and simulate hardware-optimized implementations of DSP algorithms**

- Algorithms use hardware-friendly control signals such as valid, reset, and backpressure signals.
- Select from hardware architecture options to quickly explore throughput and resource tradeoffs.
- Model realistic pipelining and latency in Simulink®.
- Algorithms such as FFT, FIR filter, decimation and interpolation, Farrow rate conversion, and NCO, are available as Simulink blocks or MATLAB® System objects.

## **Enable gigasamples-per-second (GSPS) throughput by using optional parallel processing**

DSP HDL Toolbox™ blocks and System objects can accept vector input and implement parallel architectures to achieve high sample throughputs with lower clock rates.

## **Generate HDL code for FPGAs, ASICs, and SoCs (requires HDL Coder)**

DSP HDL Toolbox algorithm implementations are optimized to fit well into DSP blocks on FPGAs and are pipelined to minimize critical path and increase synthesized clock frequency.